

13. (Amended) A transistor as recited in claim 12, [said process including further steps of

removing said] the dielectric layer having been removed, and [forming] comprising source and drain impurity regions formed adjacent said gate structure.

14. (Amended) A transistor as recited in claim 13, [wherein said step of forming] said source and drain impurity regions having been formed [is performed] by impurity implantation.

15. (Amended) A transistor as recited in claim 13, [said process including a further step of] including

[depositing] an insulator layer deposited over said source and drain regions and said gate structure.

16. (Amended) A transistor as recited in claim 15, [said process including a further step of planarizing said] wherein the insulator layer is planarized to said gate structure.

17. (Amended) A transistor as recited in claim 12, wherein said gate [location] is [defined] between source and drain impurity regions.

18. (Amended) A transistor as recited in claim 17, [said process including a further step of] wherein [planarizing] said gate structure is planarized to said dielectric layer.

19. (Amended) A transistor as recited in claim 12, wherein [said step of supplying] impurities were supplied [is performed] by angled implantation within said trench.